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November 1, 1999

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No.: 1001-0062

Transmitted herewith for filing is a patent application as follows:

Inventor(s): Dennis James Herrell
Title: CROSSTALK CANCELLATION FOR INTEGRATED CIRCUIT PACKAGE
CONFIGURATION

Enclosed are:

- 16 Pages of Specification (including Written Description, Claims and Abstract)
- 6 Sheets of Drawings, ☐ Formal / ☒ Informal
- ☒ Declaration for Patent Application (2 pages), ☒ Executed / ☐ Unexecuted
- ☒ Assignment of the Invention (3 pages, including Cover Sheet)
- ☐ Information Disclosure Statement (____ pages)
☐ with Form(s) PTO 1449 (____ page(s)) and copies of ____ reference(s)
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CLAIMS AS FILED

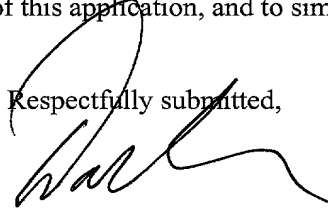
	Number Filed	Number Extra	Rate	Fee
Basic Fee =				760.00
Total Claims	22 - 20	= 2	x \$18.00 =	36.00
Independent Claims	3 - 3	= 0	x \$78.00 =	0.00
Multiple Dependent Claims (if any) - \$260.00 fee				0.00
Other: N/A				0.00
TOTAL FILING FEE				\$ 796.00

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EXPRESS MAIL LABEL NO.:

EL329123888US

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CROSSTALK CANCELLATION FOR INTEGRATED CIRCUIT PACKAGE CONFIGURATION

Dennis J. Herrell

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to maintaining signal integrity in electrical assemblies, and more particularly to a crosstalk cancellation technique suitable for integrated circuit packaging configurations.

Description of the Related Art

As semiconductor packaging densities increase, crosstalk between adjacent signal paths becomes an important noise factor that can limit performance of packaged integrated circuits. In particular, as high performance integrated circuits demand larger currents at higher frequencies with lower power supply voltages, inductively coupled crosstalk between adjacent signal paths (e.g., between pins or solder balls) may be sufficient to cause logic errors or necessitate noise tolerant circuit techniques. Accordingly, techniques are desired whereby the effects of crosstalk between adjacent signal paths, e.g., between adjacent signal paths in a Pin Grid Array (PGA), Ball Grid Array (BGA), etc., may be reduced.

One commonly used technique for canceling crosstalk in data connectors includes use of antiphase signal pairs and the cancellation of a primary crosstalk signal coupled from a first signal path of the pair using an antiphase crosstalk signal coupled from the second signal path of the pair. U.S. Patent 5,679,027 describes one such technique applied to an RJ45 connecting system of plugs and jacks by exploiting capacitive coupling of conductors. U.S. Patent 5,547,405 a similar approach to suppression of crosstalk in a telecommunications connector. Such techniques have also been employed in integrated circuit signal line systems such as differential bit line pairs of a semiconductor memory as shown in U.S. Patent 5,475,643.

However, unlike telecommunications connectors and differential bit-line circuit designs, differential signal pairs are typically not available in semiconductor packaging configurations. As a result, crosstalk suppression techniques relying on equal and opposing coupling of antiphase voltages onto a signal line are inapposite.

5 Furthermore, in many high performance packaged integrated circuit applications, inductively coupled crosstalk is dominant. Accordingly, other techniques are needed to address crosstalk issues presented by high-density semiconductor packaging technologies.

SUMMARY OF THE INVENTION

10 A technique has been developed whereby crosstalk induced in a first electrical connection by current flow at an adjacent second electrical connection is at least partially cancelled by an opposing crosstalk signal induced at an inductive coupling between electrical traces extending from or toward the first and second electrical connections, respectively. Crosstalk cancellation is provided by orienting the
15 electrical traces such that current flow through the second electrical connection and respective electrical trace induces an opposing crosstalk signal at the inductive coupling. In some configurations, an inductive coupling between electrical traces includes essentially parallel portions of the traces and an aperture in a voltage plane.

Configurations are described wherein cancellation of crosstalk induced by
20 multiple adjacent electrical connection is provided. In various configurations, crosstalk inducing electrical connections include pins, solder bumps, leads, wires, edge connectors, etc. In various configurations, crosstalk cancellation is provided on a board, on a semiconductor package, or on a semiconductor integrated circuit. The crosstalk inducing electrical connections may be integral with the board, package or
25 integrated circuit or may be mated therewith. Accordingly, a variety of configurations are envisioned including manufacturing precursors with and without the crosstalk inducing electrical connections.

In one embodiment in accordance with the present invention, an electrical assembly includes traces extending toward respective off-assembly connections.
30 Integrated transformer structures are defined along the traces to induce compensating crosstalk signals having opposing polarity to initial crosstalk signals associated with

mutual coupling between adjacent of the off-assembly connections. In some realizations, one or more of the integrated transformer structures include an aperture in a voltage plane of the electrical assembly and essentially parallel portions of corresponding pairs of the traces. The essentially parallel portions traverse, or pass over, the aperture. In various realizations, the electrical assembly includes an integrated circuit chip, a chip carrier or package, or a board or card and the off-assembly connections include pins, solder joints, leads, or wires.

In another embodiment in accordance with the present invention, a crosstalk compensation circuit for offsetting an original crosstalk signal induced at a first off-assembly connection by one or more signals on one or more adjacent off-assembly connections includes electrical traces respectively coupled to the first and adjacent connections. The electrical traces traverse apertures defined in one or more voltage planes of the assembly to inductively couple compensating crosstalk signals having opposing polarity to the original crosstalk signal.

In yet another embodiment in accordance with the present invention, a method of canceling crosstalk introduced at a first electrical connection to a packaged integrated circuit by signals on an adjacent one or more electrical connections thereto includes defining a first signal trace from the first electrical connection and respective second signal traces from the adjacent electrical connections, and defining transformer structures. The transformer structures inductively couple respective of the second signal traces to the first signal trace and are matched to induce signals substantially canceling the crosstalk introduced at the first electrical connection.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

FIG. 1 depicts a crosstalk cancellation configuration in accordance with an embodiment of the present invention wherein cancellation is provided for crosstalk signals induced at a given electrical connection by two immediately adjacent electrical connections.

FIG. 2 depicts a circuit representation corresponding to the embodiment of **FIG. 1**.

FIG. 3 depicts an electrical simulation model for two inductively coupled electrical connections and a crosstalk cancellation configuration in accordance with the present invention.

FIG. 4 illustrates coupling of a crosstalk signal from one of the two inductively coupled electrical connections in the simulation model of **FIG. 3** to the other without crosstalk cancellation.

FIG. 5 illustrates cancellation, in accordance with the present invention, of a crosstalk signal induced from one to the other of the two inductively coupled electrical connections in the simulation model of **FIG. 3**.

FIG. 6 overlays the uncanceled signal of **FIG. 4** and the canceled signal of **FIG. 5** to emphasize the efficacy of the crosstalk cancellation technique.

The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

FIG. 1 illustrates a crosstalk cancellation configuration in accordance with one embodiment of the present invention, wherein cancellation is provided for crosstalk signals induced at a given electrical connection by two immediately adjacent electrical connections. Electrical connections **1**, **2**, **3**, **4**, and **5** are illustrative of any form of electrical connection at which a crosstalk signal may be induced by current flow in a neighboring electrical connection. For example, in one illustrative exploitation, crosstalk cancellation configuration **100** is disposed on an integrated circuit package and electrical connections **1-5** include pins, leads, solder balls, or other electrical connections off the integrated circuit package. Electrical connections **1-5** may connect the integrated circuit package to a higher level package such as a board or card, or may connect the integrated circuit package to a lower level package or article such as an integrated circuit die.

Operation of crosstalk cancellation configuration **100** is now described in the context of a subset of electrical connections and associated traces illustrated in **FIG. 1**. Nonetheless, based on the description herein, persons of ordinary skill in the art will appreciate application of the techniques to the remaining electrical connections and associated traces. Furthermore, although particular types of electrical connections and particular electrical assembly configurations are described, such description is for illustration of the principles of the invention only and the illustrative electrical connection types and electrical assembly configurations shall not be taken as limiting. Indeed, based on the description herein, persons of ordinary skill in the art will appreciate applications to a variety of electrical assemblies, including but not limited to packaged integrated circuit applications.

Referring then to **FIG. 1**, crosstalk induced at electrical connection **3** by current flowing through adjacent electrical connection **2** and **4** is at least partially cancelled using integrated transformer structures **110B** and **110C**. In particular, because of the orientation of trace **123** (through which connection **2** currents flow) with respect to trace **121** (through which connection **3** currents flow), the connection **2** related component of crosstalk inductively coupled into trace **121** at connection **3** is largely cancelled by opposing crosstalk inductively coupled into trace **121** at integrated transformer structure **110B**. Similarly, because of the orientation of trace **122** (through which connection **4** currents flow) with respect to trace **121** (through which connection **3** currents flow), the connection **4** related component of crosstalk inductively coupled into trace **121** at connection **3** is largely cancelled by opposing crosstalk inductively coupled into trace **121** at integrated transformer structure **110C**.

Of course, in the illustrated configuration, crosstalk is coupled from connection **3** into connections **2** and **4** as well as *vice versa*. Therefore, of note, integrated transformer structure **110B** also provides crosstalk cancellation with respect to currents induced at electrical connection **2** by current flow through electrical connection **3** and integrated transformer structure **110C** also provides crosstalk cancellation with respect to currents induced at electrical connection **4** by current flow through electrical connection **3**. In the same manner, integrated transformer structure **110A** provides crosstalk cancellation for currents induced between electrical connections **1** and **2** and integrated transformer structure **110D**

provides cancellation for crosstalk induced between electrical connections 4 and 5. Additional integrated transformer structures 110 illustrate application of the crosstalk cancellation technique to additional electrical connections.

Although the design of transformer structures suitable to a given electrical assembly may vary depending on the characteristics or design of a particular electrical assembly, one advantageous configuration is particularly suitable for definition on a planar electrical assembly (e.g., on a board, card, package, or integrated circuit chip). In such configurations, a voltage plane is generally employed to reduce inductive coupling between traces on the electrical assembly. In one realization, apertures are defined in the voltage plane to provide the integrated transformer structures 110, 110A, 110B, 110C, and 110D. By orienting corresponding ones of the electrical traces (e.g., electrical traces 121, 122, 123, etc.) to traverse the apertures such that the relative direction of current flows therethrough opposes that through neighboring ones of the electrical connections, compensating and opposing crosstalk signals may be induced at the integrated transformer structures to provide crosstalk cancellation. In some configurations, electrical traces (e.g., 121, 122, 123, etc.) may be defined over (or under) an opening in the voltage plane below (or above). In other configurations, the electrical traces may be defined coplanar with the voltage plane and simply traverse in apertures defined therein. In such configurations, electrical traces and voltage planes may be formed using any suitable conventional process. Materials (such as metals, doped poly-silicon, etc.) suitable for a particular electrical assembly will be appreciated by persons of ordinary skill in the art.

In general, individual integrated transformer structures should be positioned as close as possible to corresponding electrical connections. Typically, electrical distances between a crosstalk inducing feature (e.g., a pair of pins or off-assembly electrical connections) and a corresponding transformer structure will be much less than a signal rise time. For example, in one realization of an electrical assembly in accordance with the present invention operating with typical off-assembly signal pulses having a pulse width of 4 ns and a rise time of 1 ns (e.g., an exemplary packaged microprocessor with a off-package 250 MHz bus interface), transformer structures would appropriately be placed within 250 ps of off-package pins. Persons of ordinary skill in the art will appreciate suitable physical distances based on the

description herein and based on particular impedance characteristics of a given implementation. Nonetheless, given typical impedance characteristics, a physical distance of perhaps half an inch may correspond to a 250 ps delay. In general, the mutual inductance afforded by a crosstalk canceling transformer structure should be of roughly the same magnitude as that of the corresponding crosstalk inducing electrical connections. For example, given a mutual inductance of 2 nH between a pair of electrical connections, the corresponding crosstalk canceling transformer structure should provide approximately 1-4 nH of compensating mutual inductance.

Although **FIG. 1** illustrates a suitable configuration for crosstalk cancellation in a array of electrical connections, e.g., a linear array, wherein the dominant crosstalk is associated with nearest neighboring electrical connections in the linear array, persons of ordinary skill in the art will appreciate extensions of the crosstalk cancellation technique to arrays of differing geometries (e.g., to two dimensional arrays), to array geometries with larger numbers of nearest neighbors, and to configurations wherein crosstalk signals may be induced at a given electrical connection by current flows through electrical connections beyond its nearest neighbors. In such configurations, additional stages of transformer structures may be defined, though with some increase in the complexity of trace routings.

FIG. 2 illustrates a circuit diagram corresponding to the crosstalk cancellation configuration of **FIG. 1**. Coupling between electrical connections 1 and 2 is illustrated as equivalent as transformer M_{12} . Similarly, respective couplings between electrical connections 2 and 3, between electrical connections 3 and 4, and between electrical connections 4 and 5 are illustrated as equivalent transformers M_{23} , M_{34} , and M_{45} , respectively. In the illustration of **FIG. 2**, circuit portion 201 includes off-assembly electrical connections and circuit portion 202 includes on-assembly crosstalk compensation structures such as those as described above.

In general, the illustrated crosstalk compensation technique may be applied to a variety of electrical assembly types, including cards, boards, semiconductor packages, integrated circuit chips, etc. Also in general, the off-assembly electrical connections may include pins, solder balls, leads, or other electrical connections susceptible to inductively coupled crosstalk. Off-assembly electrical connections

may, in general, be to a higher-level or lower-level electrical assembly. For example, in an exemplary realization of the illustrated technique on an integrated circuit package, circuit portion **202** is defined on-package to cancel crosstalk induced at off-package connections such as pins, solder balls, leads, etc. to a card, board, or other higher-level package. In an exemplary variation, off-package connections may include electrical connections to a lower-level assembly, e.g., pins, solder balls, leads, etc. to an integrated circuit chip or other lower-level assembly. Realizations of the illustrated technique to other electrical assembly types, e.g., cards, boards, integrated circuit chips, etc. may similarly compensate for crosstalk induced at off-assembly connections to higher-level or to lower-level electrical assemblies.

Some embodiments in accordance with the present invention need not include off-assembly circuit portion **201**. For example in some configurations, on-assembly circuit portion **202** is defined to provide crosstalk cancellation once off-assembly electrical connections are defined, formed, or connected thereto. In such a configuration, embodiments in accordance with the present invention are matched to crosstalk characteristics of yet to be formed or connected off-assembly electrical connections.

FIG. 3 illustrates a circuit model by which advantages of a crosstalk cancellation configuration in accordance with the present invention have been illustrated using simulation. In the illustration of **FIG. 3**, transformer **301** models the mutual inductance between a pair of adjacent off-assembly electrical connections (e.g., between electrical connections **1** and **2** of **FIGS. 1** and **2**) and transformer **302** models an integrated transformer structure defined on-assembly (e.g., integrated transformer structure **110A**). Other aspects of lossy transmission lines are modeled as shown in **FIG. 3**. When one electrical connection, e.g., electrical connection **1'**, is driven with a periodic signal, a crosstalk signal will be induced at an adjacent electrical connection, e.g., at electrical connection **2'**, by virtue of the mutual inductance therebetween, which in the illustration of **FIG. 3** is modeled as transformer **301**.

FIG. 4 illustrates results of a simulation modeling such crosstalk without benefit of the crosstalk cancellation technique described herein. In particular, **FIG. 4**

illustrates a crosstalk component **401** impressed on an otherwise quiescent signal by current flow through an adjacent connector corresponding to periodic signal **402**. In the context of **FIG. 3**, periodic signal **402** corresponds to a voltage measured across capacitor **C47**. The crosstalk component **401** impressed on an otherwise quiescent signal corresponds to a voltage measured across resistance **RI**. The simulation results presented in **FIG. 4** correspond to results of a simulation in which transformer **302** is omitted, i.e., in which on-assembly inductive coupling and associated parasitic capacitance **C44** are not included. In this way, the simulation results are illustrative of a configuration without crosstalk cancellation in accordance with the present invention.

In contrast, **FIG. 5** illustrates the efficacy of crosstalk cancellation configurations in accordance with the present invention. In particular, **FIG. 5** illustrates a substantially reduced crosstalk component **501** impressed on an otherwise quiescent signal by current flow through an adjacent connector corresponding to periodic signal **402**. As before, periodic signal **402** corresponds to a voltage measured across capacitor **C42**. Also as before, the crosstalk component **501** impressed on an otherwise quiescent signal corresponds to a voltage measured across resistance **RI**. Simulation results presented in **FIG. 4** correspond to results of a simulation in which transformer **302** is *included*, i.e., in which on-assembly inductive coupling is employed to suppress crosstalk induced at an off-assembly electrical connection **2'** by current flow through adjacent off-assembly electrical connection **1'**. **FIG. 6** overlays a portion of traces **401** and **501** to emphasize the efficacy of crosstalk cancellation configurations in accordance with the present invention. In particular, peak crosstalk induced excursions impressed on the otherwise quiescent signal are reduced from approximately 85 mV to approximately 15 mV.

While the invention has been described with reference to various embodiments, it will be understood that these embodiments are illustrative and that the scope of the invention is not limited to them. Many variations, modifications, additions, and improvements of or to the embodiments described are possible. For example, although simulation results illustrate the efficacy of a crosstalk cancellation configuration suitable to a single isolated pair of electrical connections and associated traces, persons of ordinary skill in the art will recognize that the modeled technique

may be applied to configurations wherein crosstalk is induced at a given off-assembly electrical connection by more than one adjacent off-assembly electrical connection.

For example, as illustrated in **FIGS. 1** and **2**, techniques described herein may be applied to configurations, wherein the dominant crosstalk is associated with inductive couplings to two nearest neighbors. One such configuration includes a linear array of off-assembly connections arrayed as peripheral pins on a semiconductor package. Similarly, persons of ordinary skill in the art will appreciate scale-up of the techniques described herein to cancellation of crosstalk induced by larger numbers of off-assembly electrical connections. For example, one such configuration includes a two-dimensional array of off-assembly connections arrayed as solder balls for connecting a semiconductor package to a board or card. In such a configuration, additional stages of integrated on-assembly transformer structures may be defined to provide crosstalk cancellations for signals induced by larger numbers of neighboring off-assembly electrical connections (e.g., for 4 nearest neighboring off-assembly electrical connections in a two-dimensional array of such connections). Note that in such a configuration, on-assembly transformer structures may be defined on the semiconductor package, on the board or card, or on both the semiconductor package and the board or card.

Configurations are also envisioned wherein crosstalk cancellation may be provided for signals induced by current flows through off-assembly electrical connections beyond those immediately adjacent to a given off-assembly electrical connection. Furthermore, although embodiments have been described primarily in the context of an integrated circuit package and off-package connections (e.g., to a lower-level assembly such as an integrated circuit chip or to a higher-level assembly such as a board or card), exploitation of the techniques described herein is not limited to the integrated circuit package. For example, crosstalk cancellation in accordance with the present invention may be performed at a variety of levels in a hierarchy of electrical assemblies. Based on the description herein, persons of ordinary skill in the art will appreciate suitable variations for other connection technologies and for combinations of connection technologies. These and other variations, modifications, additions, and improvements may fall within the scope of the invention as defined in the claims

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which follow and will be appreciated by persons of ordinary skill in the art based on the description herein.

WHAT IS CLAIMED IS:

1 1. An electrical assembly comprising:
2 traces extending toward respective off-assembly connections; and
3 integrated transformer structures defined along the traces to induce
4 compensating crosstalk signals having opposing polarity to initial
5 crosstalk signals associated with mutual coupling between adjacent of
6 the off-assembly connections.

1 2. The electrical assembly of claim 1, wherein one or more of the integrated
2 transformer structures each comprise:
3 an aperture in a voltage plane of the electrical assembly;
4 essentially parallel portions of corresponding pairs of the traces, the essentially
5 parallel portions passing over the aperture.

1 3. The electrical assembly of claim 1, wherein one or more of the integrated
2 transformer structures each comprise:
3 an aperture in a voltage plane of the electrical assembly; and
4 essentially parallel portions of corresponding pairs of the traces, the essentially
5 parallel portions coplanar with the voltage plane and traversing the
6 aperture therein.

1 4. The electrical assembly of claim 1, further comprising:
2 the off-assembly connections.

1 5. The electrical assembly of claim 1, including a semiconductor package,
2 wherein the off-assembly connections include pins, solder connections, leads,
3 or wires; and
4 wherein the traces are formed on the semiconductor package.

1 6. The electrical assembly of claim 1, including a board or card,
2 wherein the off-assembly connections include pins or leads of a semiconductor
3 package or solder connections or wires thereto; and
4 wherein the traces are formed on the board or card.

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1 7. The electrical assembly of claim 1, including a board or card,
2 wherein the off-assembly connections include pins, leads, solder connections
3 or edge connectors; and
4 wherein the traces are formed on the board or card.

1 8. The electrical assembly of claim 1, including a semiconductor package,
2 wherein the off-assembly connections include pins, solder connections, leads,
3 or wires.

1 9. The electrical assembly of claim 1,
2 wherein the traces and the off-assembly connections are on opposing sides of
3 the electrical assembly; and
4 wherein an electrical connection between a trace and a respective off-assembly
5 connection includes a plated through hole or conductive via.

1 10. The electrical assembly of claim 1,
2 wherein the off-assembly connections are organized as an array thereof; and
3 wherein, for each of the traces, one or more of the integrated transformer
4 structures are defined therealong to induce respective of the
5 compensating crosstalk signals and thereby oppose respective of the
6 initial crosstalk signals introduced at a corresponding one of the off-
7 assembly connections by nearest neighbors thereof.

1 11. The electrical assembly of claim 10,
2 wherein the array includes a linear array;
3 wherein the nearest neighbors number two; and
4 wherein, for essentially each of the traces, two of the integrated transformer
5 structures are defined therealong to induce respective of the
6 compensating crosstalk signals and thereby oppose respective of the
7 initial crosstalk signals introduced by the nearest neighbors.

1 12. The electrical assembly of claim 1,

2 wherein the off-assembly connections include one of pins, solder joints, leads,
3 and wires.

1 13. The electrical assembly of claim 1, wherein the electrical assembly
2 includes an integrated circuit chip.

1 14. The electrical assembly of claim 1, wherein the electrical assembly
2 includes a chip carrier or package.

1 15. The electrical assembly of claim 1, wherein the electrical assembly
2 includes a board or card.

1 16. A crosstalk compensation circuit for offsetting an original crosstalk signal
2 induced at a first off-assembly connection by one or more signals on one or more
3 adjacent off-assembly connections, the crosstalk compensation circuit comprising:
4 electrical traces respectively coupled to the first and adjacent connections; and
5 the electrical traces traversing apertures defined in one or more voltage planes
6 of the assembly to inductively couple compensating crosstalk signals
7 having opposing polarity to the original crosstalk signal.

1 17. The crosstalk compensation circuit of claim 16,
2 wherein the assembly includes a semiconductor package; and
3 wherein the first and adjacent connections are to a board or card.

1 18. The crosstalk compensation circuit of claim 16,
2 wherein the assembly includes a semiconductor package; and
3 wherein the first and adjacent connections are to an integrated circuit chip.

1 19. A method of making a circuit for canceling crosstalk introduced at a first
2 electrical connection to a packaged integrated circuit by signals on an adjacent one or
3 more electrical connections thereto, the method comprising:
4 defining a first signal trace from the first electrical connection and respective
5 one or more second signal traces from the adjacent one or more
6 electrical connections; and

7 defining one or more transformer structures, the transformer structures
 8 inductively coupling respective of the one or more second signal traces
 9 to the first signal trace, the transformer structures matched to induce
 10 signals substantially canceling the crosstalk introduced at the first
 11 electrical connection.

1 20. A method as in claim 19,
 2 wherein the first signal trace, the second signal traces and the transformer
 3 structures are defined as part of the packaged integrated circuit.

1 21. A method as in claim 19,
 2 wherein the first signal trace, the second signal traces and the transformer
 3 structures are defined as part of a board or card to which the packaged
 4 integrated circuit is connectable using the first and adjacent electrical
 5 connections.

1 22. A method as in claim 19, wherein for each transformer structure, the
 2 defining includes:
 3 defining an aperture in a voltage plane of the integrated circuit chip; and
 4 orienting the first signal trace and one of the second signal traces to define
 5 substantially parallel portions thereof traversing at least a portion of the
 6 aperture.

CROSSTALK CANCELLATION FOR INTEGRATED CIRCUIT PACKAGE CONFIGURATION

Dennis J. Herrell

ABSTRACT OF THE DISCLOSURE

5 A technique has been developed whereby crosstalk induced in a first electrical connection by current flow at an adjacent second electrical connection is at least partially cancelled by an opposing crosstalk signal induced at an inductive coupling between electrical traces extending from or toward the first and second electrical connections, respectively. Crosstalk cancellation is provided by orienting the

10 electrical traces such that current flow through the second electrical connection and respective electrical trace induces an opposing crosstalk signal at the inductive coupling. In some configurations, an inductive coupling between electrical traces includes essentially parallel portions of the traces and an aperture in a voltage plane. In some configurations, cancellation of crosstalk induced by multiple adjacent

15 electrical connection is provided. Crosstalk inducing electrical connections include pins, solder bumps, leads, wires, edge connectors, etc. In various configurations, crosstalk cancellation is provided on a board, on a semiconductor package, or on a semiconductor integrated circuit. The crosstalk inducing electrical connections may be integral with the board, package or integrated circuit or may be mated therewith.

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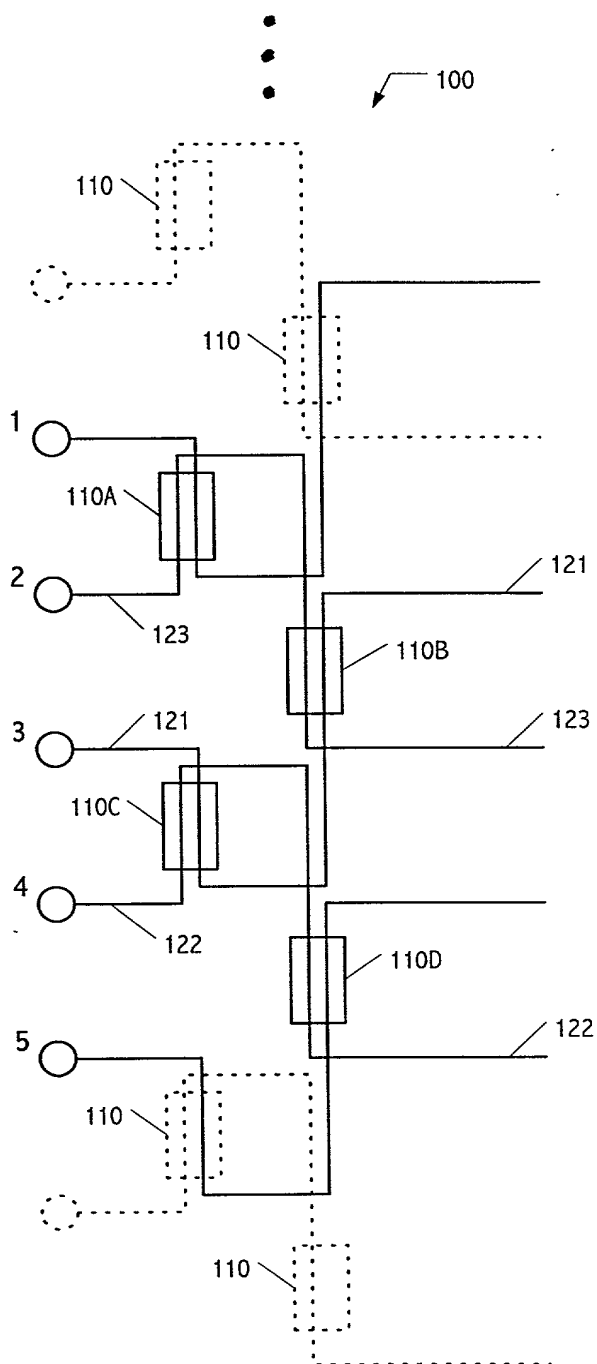


FIG. 1

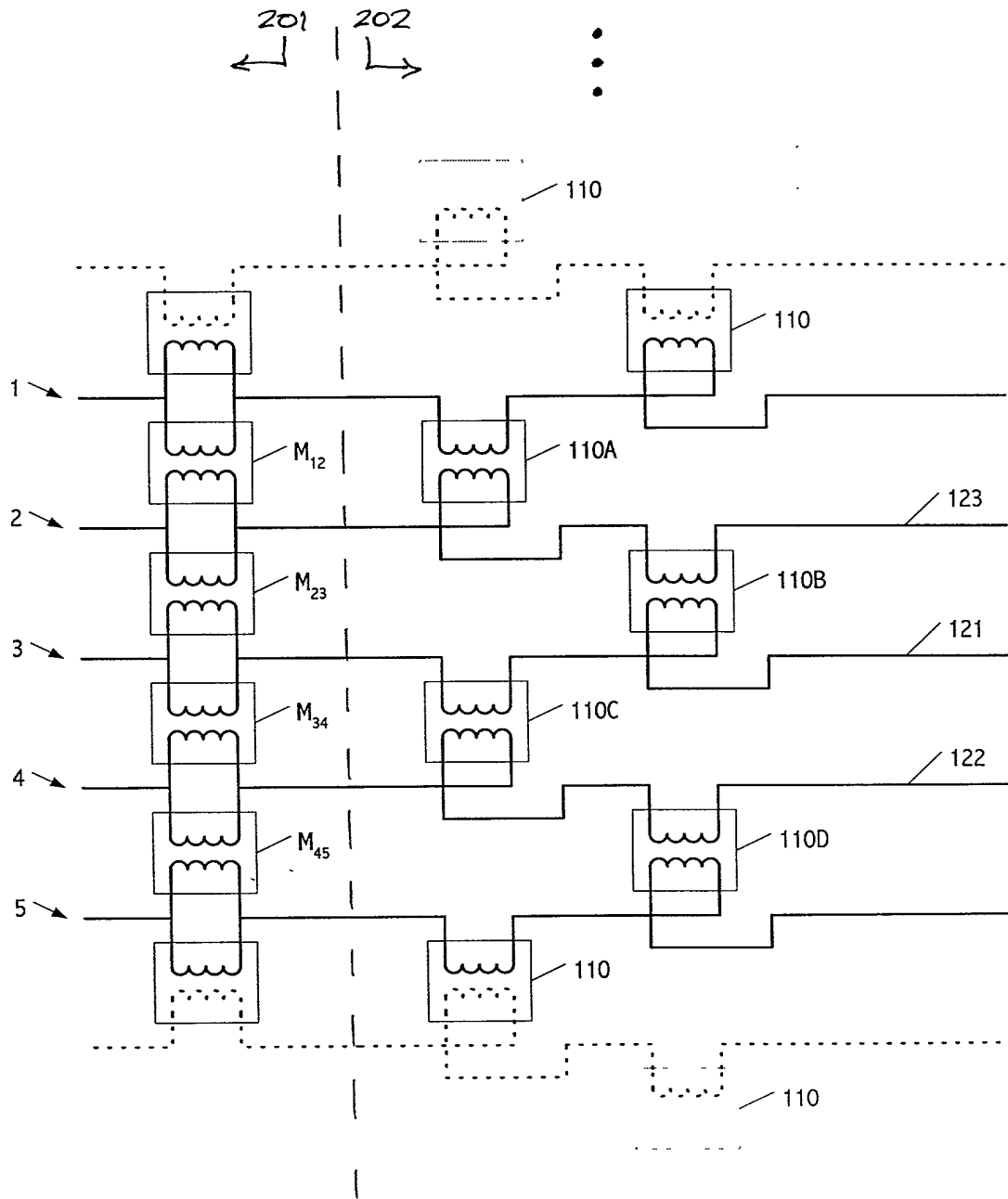


FIG. 2

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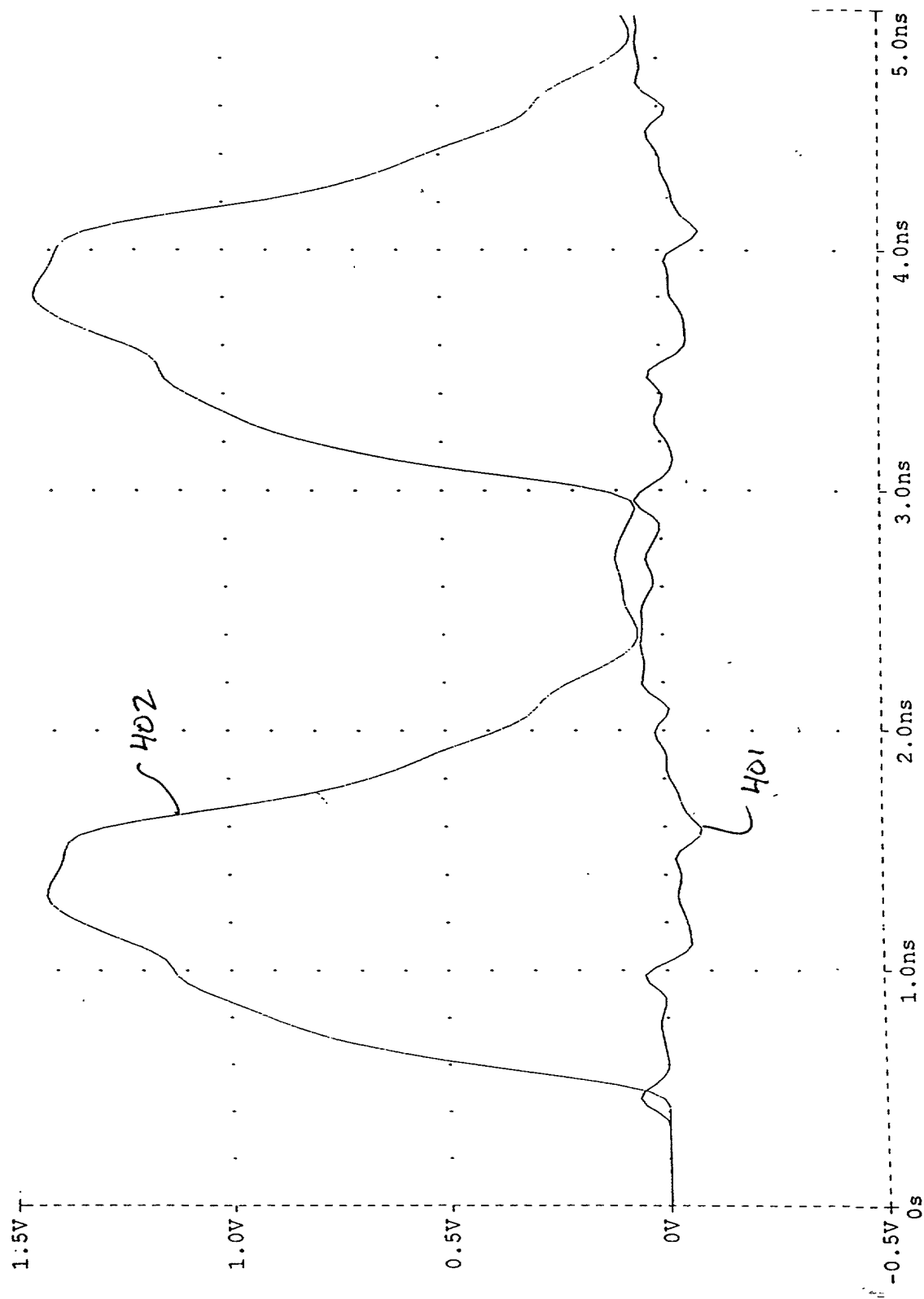


FIG. 4

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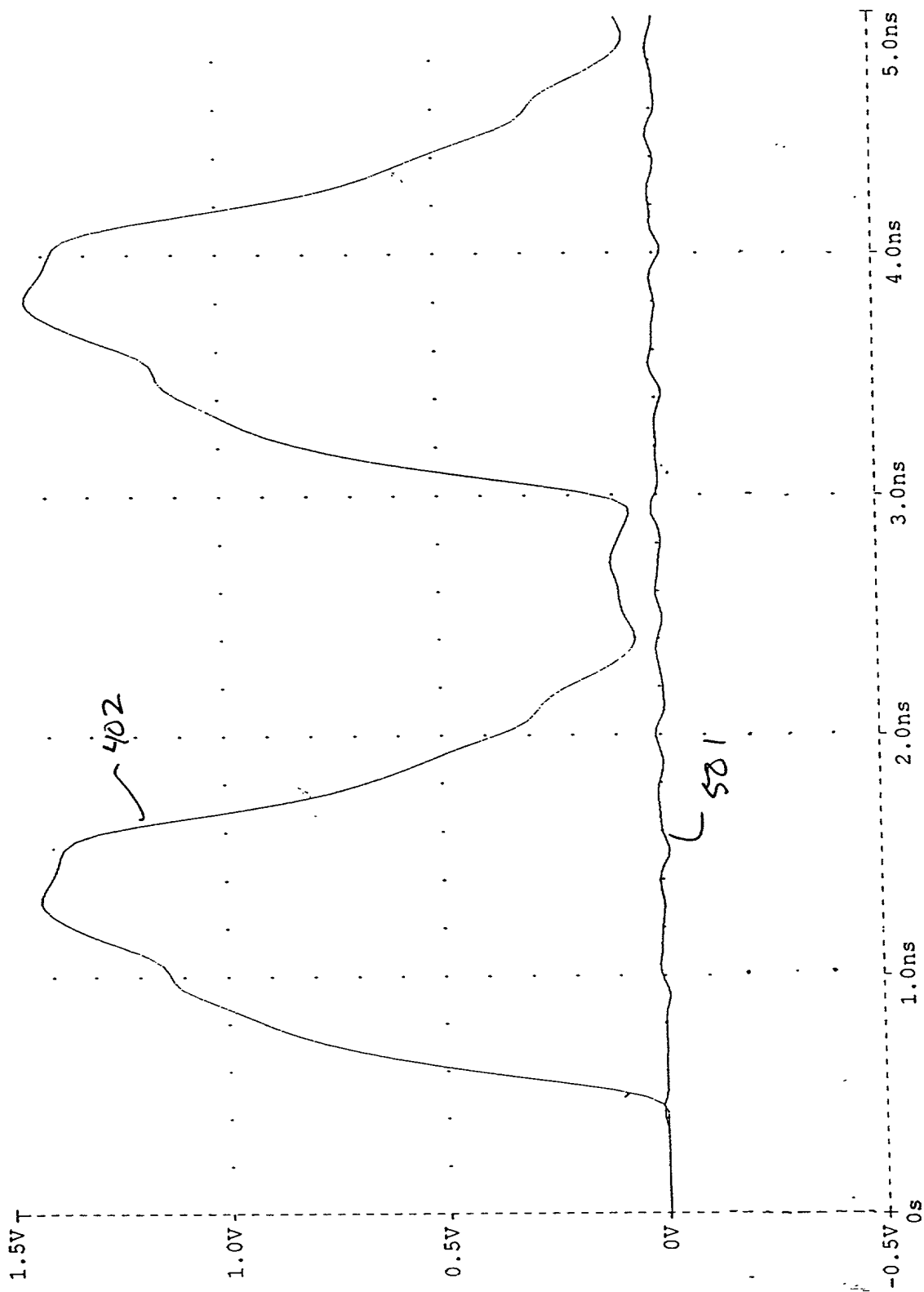


FIG. 5

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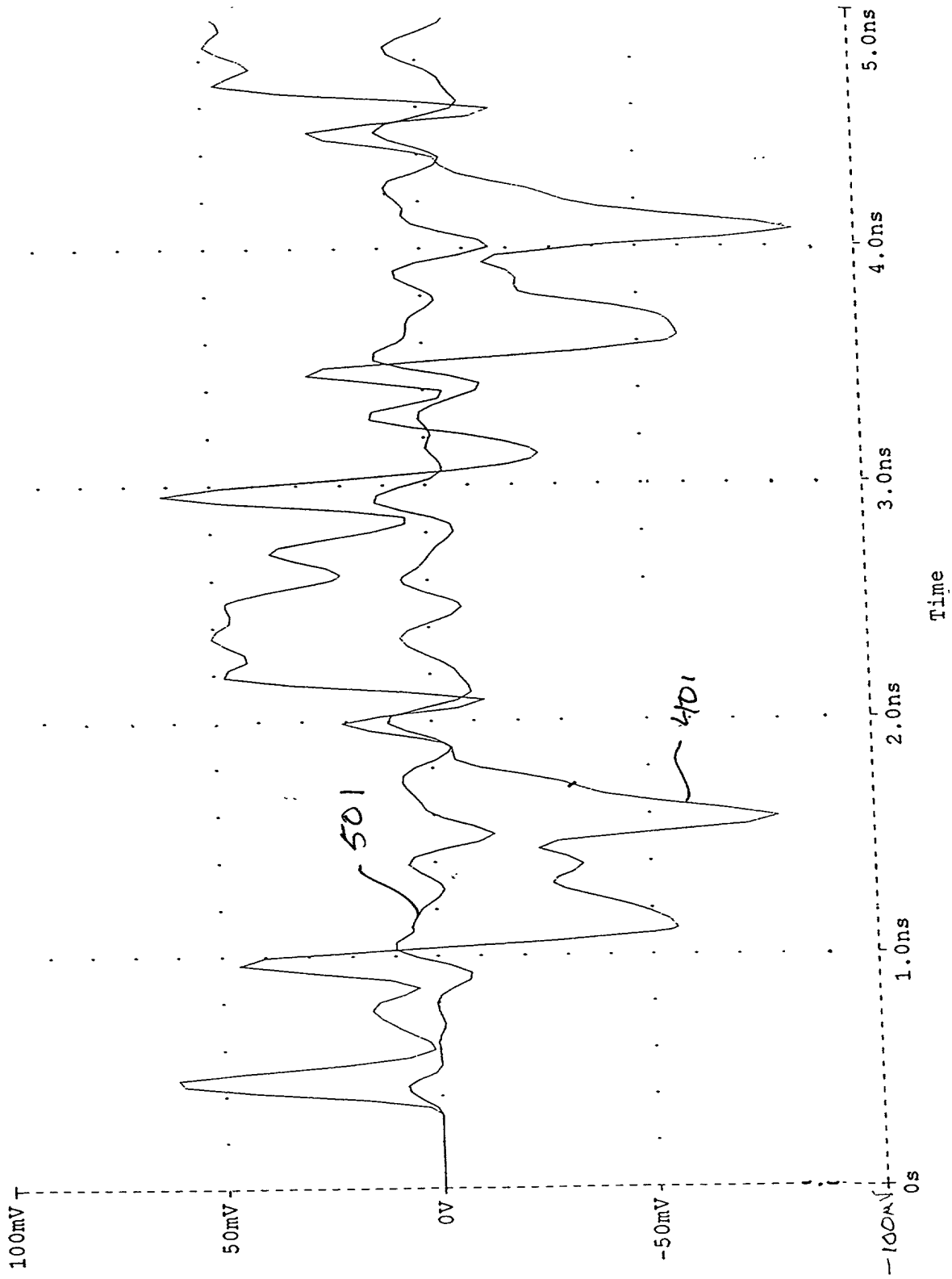


FIG. 6

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

CROSSTALK CANCELLATION FOR INTEGRATED CIRCUIT PACKAGE CONFIGURATION

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A				

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

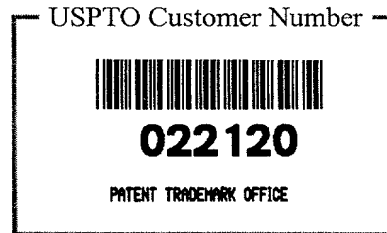
I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Mark Zagorin (36,067); Andrew C. Graham (36,531); David W. O'Brien (40,107); Paul S. Drake (33,491); Vincenzo D. Pitruzzella (28,656); Louis A. Riley (39,817); William D. Zahrt, II (26,070); Richard J. Roddy (27,688); and Elizabeth A. Apperley (36,428).

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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